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PATENT APPLICATION

SYSTEM AND METHOD OF DETECTING ROTATED DISPLAYS

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SYSTEM AND METHOD OF DETECTING ROTATED DISPLAYS

BACKGROUND OF THE INVENTION

[0001] The present invention relates generally to detecting a rotation, and other state changes, of a display, and particularly to adjusting an image displayed by the display. The prior art includes displays that rotate. Typically, user intervention and/or dedicated signal lines are required to respond to the rotation of a display. For example, if a user rotates a display, the user may also be required to manually notify the source of imagery displayed by the display (e.g., a computer) about the rotation. In some prior art systems, manually notifying the source of the imagery may include pressing one or more keys of a keyboard connected to the source. Upon detecting this action, the source may rotate the imagery to match the rotation of the display. In still other prior art systems, the display detects rotations and notifies the source without user intervention, but uses dedicated lines connected to the source to notify the source about display rotations.

[0002] What is needed in the art, therefore, is a system and method for detecting display rotations and notifying the source of imagery displayed by the display about the display rotations that does not require a set of dedicated lines.

BRIEF SUMMARY OF THE INVENTION

[0003] A system for adjusting display data orientation. The system includes graphics circuitry to send and receive control signals over a set of control lines. The exchange of control signals is governed by a communication protocol. The graphics circuitry is configured to request orientation information via the set of control lines upon detecting a modulation of the set of control lines that is undefined by or illegal under the communication protocol. Based on the orientation information received in response to the request, the graphics circuitry adjusts the orientation of display data transmitted by the graphics circuitry.

[0004] A system for processing orientation changes. The system includes a display device configured to communicate over a set of control lines in accordance with a communication protocol. The display device is further configured to detect changes to its orientation. The display device is also configured to initiate a modulation of the set of control lines that is undefined by or illegal under the communication protocol upon making such a detection.

[0005] A system for processing display device orientation changes. This system includes a display device and graphics circuitry. These two devices are configured to exchange control signals over a set of control lines in accordance with a communication protocol. The display device is further configured to detect a change in its orientation. In response to such a
5 detection, the display device is configured to initiate a modulation of the set of control lines that is undefined by or illegal under the communication protocol. The graphics circuitry is further configured to request orientation information from the display device upon detecting the modulation of the set of control lines. Finally, the graphics circuitry is configured to adjust the orientation of display data transmitted to the display device by reference to the
10 orientation information received from the display device via the set of control lines.

[0006] A system for adjusting display data orientation. The system includes graphics circuitry to send and receive control signals over a set of control lines. The exchange of control signals is governed by a master/slave communication protocol under which the graphics circuitry is a lone master of the set of control lines. The graphics circuitry is
15 configured to request orientation information via the set of control lines upon detecting a modulation of the set of control lines that is undefined by the master/slave communication protocol and not initiated by the graphics circuitry. Based on the orientation information received in response to the request, the graphics circuitry adjusts the orientation of display data transmitted by the graphics circuitry. A system for processing orientation changes. The
20 system includes a display device configured to communicate over a set of control lines in accordance with a master/slave communication protocol under which the display device is a slave. The display device is further configured to detect changes to its orientation. The display device is also configured to initiate a modulation of the set of control lines in violation of master/slave communication protocol upon making such a detection.

25 [0007] A system for processing display device orientation changes. The system includes a display device and graphics circuitry that are configured to exchange control signals over a set of control lines. The exchange is governed by a master/slave communication protocol under which the graphics circuitry is a lone master of the set of control lines and the display device is a slave of the set of control lines. The display device is further configured to detect
30 a change in its orientation. The display device is further configured to initiate a modulation of the set of control lines in violation of the master/slave communication protocol upon detecting the change in its orientation. The graphics circuitry is further configured to request orientation information from the display device upon detecting the modulation of the set of

control lines. Finally, the graphics circuitry is configured to adjust an orientation of display data transmitted to the display device by reference to the orientation information received via the set of control lines in response to the request.

[0008] A communication channel comprising a data signal and a clock signal. A start

5 condition is indicated on the communication channel by a high-to-low transition of the data signal followed by a high-to-low transition of the clock signal. A stop condition is indicated on the communication channel by a low-to-high transition of the clock signal followed by a low-to-high transition of the data signal. A bit value of one is indicated on the communication channel by the data signal being high while the clock signal has a low-to-high transition followed by a high-to-low transition. A bit value of zero is indicated on the communication channel by the data signal being low while the clock signal has a low-to-high transition followed by a high-to-low transition. And a state change in a slave of the communication channel is indicated on the communication channel by a pulse of the data signal while the clock signal is unchanged.

10 [0009] A communication channel consisting of a serial data line (SDA) and a serial clock line (SCL). A start condition is indicated on the communication channel by a high-to-low transition on the SDA followed by a high-to-low transition on the SCL. A stop condition is indicated on the communication channel by a low-to-high transition on the SCL followed by a low-to-high transition on the SDA. A bit value of one is indicated on the communication

15 channel by the SDA being high while the SCL has a low-to-high transition followed by a high-to-low transition. A bit value of zero is indicated on the communication channel by the SDA being low while the SCL has a low-to-high transition followed by a high-to-low transition. And a state change in a slave of the communication channel is indicated on the communication channel by a pulse on the SDA while the SCL is unchanged.

20 [0010] A communication channel between a master device and a slave device that includes an I²C bus with a serial data line (SDA) and a serial clock line (SCL). The slave device is configured to indicate a monitor rotation to the master device by changing a state on the SDA while the SCL is in a high state.

25 [0011] A communication channel between a master device and a slave device that includes an I²C bus with a serial data line (SDA) and a serial clock line (SCL). The slave device is configured to indicate a state change of the slave device to the master device by changing a state on the SDA while the SCL is in a high state.

[0012] A protocol for use with a two-line serial bus that includes a start condition; a stop condition; a bit with a value of one; a bit with a value of zero; and a state change condition indicating to a master device connected to the serial bus a changed state of a slave device connected to the serial bus.

5 [0013] A computer system comprising a graphics circuit, a display, and a serial bus. The graphics circuit is configured to generate display data and the display configured to display the display data. Further, the display and the graphics circuit are coupled via the serial bus, which comprises a serial data line and a serial clock line, to exchange control signals. The control signals include a start condition, which is indicated by a high-to-low transition on the serial data line followed by a high-to-low transition on the serial clock line, a stop condition, which is indicated by a low-to-high transition on the serial clock line followed by a low-to-high transition on the serial data line, a bit value of one, which is indicated by the serial data line being high while the serial clock line has a low-to-high transition followed by a high-to-low transition, a bit value of zero, which is indicated by the serial data line being low while the serial clock line has a low-to-high transition followed by a high-to-low transition, and a state change in the display, which is indicated by the display with a pulse on the serial data line while the serial clock line is unchanged.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Additional objects and features of the invention will be more readily apparent from 20 the following detailed description and appended claims when taken in conjunction with the drawings, in which:

[0015] Figure 1A illustrates a frontal view of a display and displayed text in a landscape orientation.

[0016] Figure 1B illustrates a side view of a display.

25 [0017] Figure 1C illustrates a frontal view of a display and displayed text being rotated from a landscape orientation.

[0018] Figure 1D illustrates a frontal view of a display in a portrait position and displayed text in a landscape orientation.

30 [0019] Figure 1E illustrates a frontal view of a display and displayed text in a portrait orientation.

[0020] Figure 1F illustrates a frontal view of a display and displayed text being rotated from a portrait orientation.

[0021] Figure 1G illustrates a frontal view of a display in a landscape position and displayed text in a portrait orientation.

5 [0022] Figure 1H is a block diagram of a display connected to graphics circuitry mounted within an electronic device.

[0023] Figure 2 is a block diagram of display components consistent with an embodiment of the present invention.

10 [0024] Figure 3 is a block diagram of graphics circuitry consistent with an embodiment of the present invention.

[0025] Figure 4 is a block diagram of an electronic device consistent with an embodiment of the present invention.

[0026] Figure 5A illustrates a start sequence consistent with an embodiment of the present invention.

15 [0027] Figure 5B illustrates a stop sequence consistent with an embodiment of the present invention.

[0028] Figure 5C illustrates a device address and read / write indicator consistent with an embodiment of the present invention.

[0029] Figure 6 illustrates a series of processing steps for detecting and responding to a display rotation that is consistent with an embodiment of the present invention.

20 [0030] Figures 7A and 7B illustrate invalid/undefined control signal sequences consistent with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0031] Referring to Figure 1A, there is shown a frontal view of a display 10. Visible components of the display 10 include a case 20, a screen 30, and a stand 40. The case 20 and/or stand 40 typically house a plurality of electronic and optical components (excluding the screen 30) that are not visible in Figure 1A but enable the display 10 to receive and display data 85 (Figure 1H) (e.g., digital or analog imagery). Some of these components are described below in connection with Figure 2. The screen 30 may be, for example, a cathode

ray tube ("CRT") or a flat-panel, which may use plasma technology or liquid crystal technology (e.g., a passive matrix liquid crystal display ("LCD"), an active matrix LCD, or a ferroelectric LCD). Other types of displays 10 are possible and within the scope of the present invention.

5 [0032] Figure 1B illustrates the display from a side view. From this view, the screen 30 is no longer visible, but a pivot 60, which allows the screen 30 and case 20 to rotate within a plane of the visible portion of the screen 30, is now visible. The pivot 60 enables a user to rotate the case 20 and screen 30 (i.e., the display 10) between, for example, a portrait orientation and a landscape orientation.

10 [0033] The display 10 preferably incorporates an orientation sensor that detects the orientation of the display 10 and when it changes. A wide variety of technologies may be used for this purpose without departing from the scope of the present invention. Preferably, when the case 20 and screen 30 are rotated to a new orientation, the orientation sensor preferably communicates the orientation of the display 10 to circuitry, which is described

15 below in connection with Figure 2, within the display 10. Generally, the user grasps the case 20 and rotates the screen. Optionally, the rotation can be done with a motor. For example, the orientation sensor may include one or more of the following components known in the art: a mercury switch; a mechanical switch; an optical encoder; an optical detector; or a shaft encoder. Other components are possible, and within the scope of the present invention. The

20 various switches and sensors can be read with general purpose input/output circuits that are in communication with a controller within the display 10.

[0034] With respect to the screen 30, a landscape orientation is one in which the length of the screen 30 along a vertical axis is shorter than the length of the screen 30 along a horizontal axis. Assuming that the display data 85 fills the entire screen 30, a landscape orientation, with respect to display data 85, is one in which the length of the display data 85 along an axis running from the top of the display data 85 to the bottom of the display data 85 is shorter than the length of the display data 85 along an axis running from one side of the display data 85 to another side of the display data 85. With respect to the screen 30, a portrait orientation is one in which the length of the screen 30 along a horizontal axis is shorter than the length of the screen 30 along a vertical axis. And with respect to display data 85, a portrait orientation is one in which the length of display data 85 along an axis running from one side of the display data 85 to another side of the display data 85 is shorter than the length

of the display data 85 along an axis running from top of the display data 85 to the bottom of the display data 85.

[0035] Referring again to Figure 1A, the display 10 and the display data 85 (e.g., the word "TEXT") are in a landscape orientation. Figure 1C shows the case 20 and the screen 30 being 5 rotated clockwise from the landscape orientation to a portrait orientation. Typically, a user manually rotates the display, but automated technology may be used as well without departing from the scope of the present invention.

[0036] Following a rotation of, for example, approximately 90 degrees, the display 10 is in a portrait orientation but the display data 85 initially remains in a landscape orientation as 10 illustrated in Figure 1D. The orientation of the display data 85 has not been changed by a source of the display data 85. As a result, the display data 85 is "sideways" as indicated by the orientation of the word "TEXT." Figure 1E illustrates the display data 85 and the display 10 following an adjustment to the orientation of the display data 85. Both the display data 85 and the display 10 are in a portrait orientation.

15 [0037] Figure 1F shows the case 20 and the screen 30 being rotated counter-clockwise from the portrait orientation to a landscape orientation. Following a rotation of approximately 90 degrees, the display 10 is in a landscape orientation but the display data 85 (e.g., the word "TEXT") remains in a portrait orientation as illustrated in Figure 1G. Following another adjustment to the orientation of the display data 85, both the display data 85 and the display 20 10 are in a landscape orientation as illustrated in Figure 1A.

[0038] As indicated above, the display 10 is typically not a source of the display data 85. Figure 1H illustrates a block diagram of the display 10, graphics circuitry 70, and an electronic device 80 such as a computer. The graphics circuitry 70 and/or the electronic device 80 generate the display data 85, which as illustrated in Figure 1H is transmitted from 25 the graphics circuitry 70 to the display 10.

[0039] The graphics circuitry 70 is typically responsible for formatting the display data 85 so that its orientation matches that of the display 10. The display data 85 can take the form of analog signals or digital signals. In some embodiments, the display data 85 corresponds to an array of pixels that may represent, for example, a "desktop" of a computer. The graphics 30 circuitry 70, in some embodiments, includes capacity for 3D graphics processing such that the array of pixels represents 3D animated graphics. Further, the array of pixels could be 1600 pixels horizontally and 1200 vertically (i.e., a "portrait" display) or 1200 pixels

horizontally and 1600 vertically (i.e., a "landscape" display). The size of the array of pixels is generally controlled by registers within the graphics circuitry 70, with the register values set by software (typically, driver software).

[0040] Also transmitted back and forth between the display 10 and the graphics circuitry 70

5 are control signals (e.g., a clock signal and a data signal) 87. These control signals 87 enable the graphics circuitry 70 and the electronic device 80 to, among other things, transmit and respond to requests for data. For example, when the orientation of the display 10 is changed (e.g., from landscape to portrait), the display 10 notifies the graphics circuitry 70 via the control signals 87 as described in detail below.

10 [0041] Referring to Figure 2, there is shown a block diagram of components that may be included in the display 10. Preferably, these components include a connector 220-1, display data processing circuitry 240, a display controller 250, display memory 260, an orientation detector 270, and user input buttons 280. Other components may be included in the display 10 without departing from the scope of the present invention.

15 [0042] In a preferred embodiment, a connector 220 is consistent with a mechanical video graphics array ("VGA") connector. As illustrated in Figure 2, the preferred connector 220 includes pins (for a male connector) or sockets (for a female connector) to exchange electrical signals (e.g., control signals 87, display data 85, power, ground, etc.) with the graphics circuitry 70. Different types of connectors 220 (e.g., Digital Visual Interface connectors,

20 Enhanced Video Connectors, Plug and Display connectors, Digital Flat Panel connectors, Low Voltage Differential Signaling Digital Interface connectors, etc.) may be used without departing from the scope of the present invention. Typically, the connector 220 provides the only means for electrically and mechanically connecting the display 10 to the graphics circuitry 70. Table 1 illustrates a preferred pin-out of the connector 220. Hereinafter, the pin description of Table 1 is assumed, but the invention can be applied to any other configuration 25 of pins and/or signal connections.

Pin/Skt 1	Red video
Pin/Skt 2	Green video
Pin/Skt 3	Blue video
Pin/Skt 4	Monitor ID bit 2
Pin/Skt 5	Return
Pin/Skt 6	Red video return
Pin/Skt 7	Green video return
Pin/Skt 8	Blue video return
Pin/Skt 9	+5 volt supply
Pin/Skt 10	Synchronization return
Pin/Skt 11	Monitor ID bit 0
Pin/Skt 12	Data signal
Pin/Skt 13	Horizontal synchronization
Pin/Skt 14	Vertical synchronization
Pin/Skt 15	Clock signal

Table 1

Most of the pins included in Table 1 are used to transmit display data 85 and signals 87 that control how the display data 85 is displayed. In prior art systems, the function of these 5 signals is well known. In order to keep the total number of wires connecting the display 10 and the graphics circuitry 70 to a minimum (as shown in the example of Table 1), such systems employ a two-wire interface (e.g., a serial clock line and a serial data line) or a communication channel for transmission of a subset of the control signals 87 (i.e., a clock signal and a data signal). The data signal and the clock signal enable communication 10 between the display 10 and the graphics circuitry 70 and/or the electronic device 80 that is compliant with the Display Data Channel 2B ("DDC2B") standard (the specification of which is incorporated herein by reference). As described in the DDC2B standard or specification, defined and/or legal states or transmissions of or through the two-wire interface, serial clock and data lines, or the communication channel include start conditions, stop conditions, bit 15 values of one, and bit values of zero.

[0043] Further, the data signal is defined by the DDC2B standard as being bi-directional, which means that the graphics circuitry 70 and the display 10 can transmit and receive a data signal (e.g., modulate the state of their respective data signal Pin/Skt 12). The clock signal, however, is defined by the DDC2B standard as being unidirectional such that only the 20 graphics circuitry 70 can transmit a clock signal (e.g., modulate the state of it's clock signal Pin/Skt 15).

[0044] There are, however, differences between the function or use of pins/sockets Pin/Skt 12 and Pin/Skt 15, which transmit the data signal and the clock signal, respectively, in the present invention and in prior art systems. Briefly, the present invention includes a modulation of the data signal and/or the clock signal that is inconsistent with start conditions, 5 stop conditions, bit values of one, and bit values of zero (or otherwise undefined or disallowed by the DDC2B standard).

[0045] Returning to Figure 2, specific components (not illustrated) that manipulate or monitor the state of the data signal Pin/Skt 12 and possibly the clock signal Pin/Skt 15 of the display's 10 connector 220 may include pull-up resistors, input buffers, transistors, tri-state 10 drivers, open collector drivers, and/or other components without departing from the scope of the present invention.

[0046] Some computer systems are "multi-headed" in that they have two or more monitors. In such systems, the clock and data signal is generally separate for the two monitors. That is, each monitor corresponds to a pair of data/clock signals. It is possible for multiple monitors 15 to share the same data/clock signals. Hereinafter, only single monitor systems will be described, but the invention can be applied to multi-monitor systems.

[0047] The display data processing circuitry 240 may be dependant upon the type of the display 10. For example, the display data processing circuitry 240 may include a preamplifier, a CRT driver, deflection circuitry, on-screen display circuitry, etc. when the 20 display 10 receives and displays display data 85 in an analog form.

[0048] The user input buttons 280 are typically used in conjunction with the on-screen display circuitry to, for example, adjust the size and position of display data 85 on the screen 30 and the brightness, contrast, and color settings of the screen 30. The onscreen display circuitry may, for example, display the size and position of display data 85 on the screen 30 25 and the brightness, contrast, and color settings of the screen 30 while these attributes are adjusted via the user input buttons 280.

[0049] The display data processing circuitry 240 receives input (e.g., R/GB display data signals) from the connector 220-1 and input (e.g., a horizontal synchronization signal, a vertical synchronization signal, control signals 87, etc.) from the controller 250. The output 30 of the display data processing circuitry 240 to the screen 30 is typically display data 85 and control signals 87.

[0050] The display controller 250 controls the operation of the display data processing circuitry 240, responds to manipulation of the user input buttons 280, and communicates with the graphics circuitry 70 and/or the electronic device 80. The display controller 250 may receive as input from the connector 220-1 a horizontal synchronization signal and a vertical synchronization signal, which control how the display data 85 is displayed, and a data signal and a clock signal, which together enable communication that adheres to the DDC2B standard.

[0051] The display memory 260, which may be incorporated in the display controller 250, stores information such as settings of the display 10 (e.g., the size and position of display data 85 on the screen 30 and the brightness, contrast, and color settings of the screen 30) and other data as described in detail below.

[0052] The display 10 includes a data interface to an orientation detector 270. In preferred embodiments, the orientation of the display 10 is in one of two orientations - landscape or portrait. If the display 10 is in a landscape orientation, the orientation detector 270 may, for example, adjust this data interface to a logic HIGH state. Conversely, if the display 10 is in a portrait orientation, the orientation detector 270 may, for example, adjust this data interface to a logic LOW state. When such action is taken, the display controller 250 may adjust related data maintained in the display memory 260 accordingly and signal the graphics circuitry 70 as described below.

[0053] Referring to Figure 3, there is shown a block diagram of components that may be included in the graphics circuitry 70. Specifically, these components include a connector 220-2, a board connector 320, video BIOS 330, RAMDAC 340, a graphics processor 350, and video memory 360.

[0054] The board connector 320 provides a means for mechanically and electrically connecting the graphics circuitry 70 to the electronic device 80. More specifically, a board connector 320 may secure the graphics circuitry 70 to the electronic device 80 and enables the graphics circuitry 70 and the electronic device 80 to exchange a plurality of separate electrical signals. The board connector 302 may be Peripheral Component Interconnect ("PCI") compliant, Accelerated Graphics Port ("AGP") compliant, which enables the graphics circuitry 70 to directly access the memory 460 (Figure 4) of the electronic device 80, or compliant with another standard. Alternatively, the graphics circuitry can take the form of an integrated circuit on a computer motherboard.

[0055] In some embodiments, the graphics circuitry 70, as Figure 3 suggests, is incorporated on a "card" that removably plugs into the electronic device 80 via the board connector 320. In these embodiments, a board connector 320, or other connector, is generally required. In other embodiments, however, the graphics circuitry 70 is built into the electronic device 80. For example, in embodiments in which the electronic device 80 is a computer, the graphics circuitry 70 may be mounted with components such as central processing units 450 (Figure 4) on a motherboard. In still other embodiments, the graphics circuitry 70 is incorporated on a card that is non-removably affixed to the electronic device 70. In either of these last sets of embodiments, the graphics circuitry 70 may communicate with the electronic device 80 via signal traces or other means and not use and/or include a board connector 320.

[0056] The video BIOS 330 may be a read only memory ("ROM") chip that includes operational firmware, graphics mode definitions, and screen fonts. The video BIOS 330 may also control how other components in the graphics circuitry 70 interact and perform diagnostic tests on the video memory 360 and I/O of the graphics circuitry 70.

[0057] The RAMDAC 340, which may be integrated into the graphics processor 350, converts digital display data 85 generated by the electronic device 80 and/or the graphics circuitry 70 to an analog signal for the display 10. For example, the RAMDAC 340 may read contents of the video memory 360 and convert it to analog R/GB signals that are sent to the display 10 through the connector 220. If the display data 85 is analog, the graphics circuitry generally includes a DAC of some type.

[0058] In some embodiments of the present invention, display data 85 is also (or instead) transmitted in a digital form to the display 10. In these embodiments of the invention, contents of the video memory 360 may be transmitted to the display 10 without the assistance 25 of the RAMDAC (e.g., in addition to the converted contents of the video memory 360). In these embodiments, two or more connectors 220, one of which supports the transmission of display data 85 in a digital form, may be included in the graphics circuitry 70. And in some embodiments, a RAMDAC 340 is not included such that the display data 85 is transmitted to the display 10 in a digital form only.

[0059] The graphics processor 350 typically controls display data resolution, color depth (possibly in conjunction with the RAMDAC 340), and aspects of rendering display data 85. In particular, the graphics processor 350 may handle bitmap transfers and painting, window

resizing and repositioning, line drawing, font scaling, and polygon drawing in hardware. The graphics processor 350 may function like a coprocessor or an accelerator. In the case of a coprocessor, the graphics processor 350 processes all graphics related tasks without assistance from the controller 450 of the electronic device 80 (Figure 4). In the case of an
5 accelerator, the graphics processor 350 processes specific graphics related tasks delegated by the controller 450 of the electronic device 80. The output of the graphics processor 350 (e.g., display data 85) is typically stored in the video memory 360 and subsequently transferred to the display 10.

10 [0060] As indicated above, the video memory 360 stores display data 85 (e.g., bitmaps that correspond to pixels of the screen 30) in a digital form. The video memory 360 may be formed by Video Ram ("VRAM"), Windows RAM ("WRAM"), EDO DRAM, SDRAM, SGRAM, or DRDRAM.

15 [0061] Specific components (not illustrated) that manipulate and monitor the state of the data signal Pin/Skt 12 and the clock signal Pin/Skt 15 of the graphic circuitry's 70 connector 220 may also include pull-up resistors, input buffers, transistors, tri-state drivers, open collector drivers, and/or other components without departing from the scope of the present invention.

20 [0062] Referring to Figure 4, there is shown a block diagram of components that may be included in the electronic device 80. The electronic device 80 typically comprises a computer, but may comprise other electronic devices as well. As illustrated in Figure 4, the electronic device 80 typically includes standard computer components such as one or more central processing units ("CPU") 450, input devices 480 (e.g., keyboard, mouse, network connections, etc.), a memory 460, and one or more board sockets 420.

25 [0063] The memory 208, which typically includes high speed random access memory as well as non-volatile storage such as disk storage, may store an operating system, program modules, and device drivers. The operating system includes procedures for handling various basic system services and for performing hardware dependent tasks. In particular, the operating system may provide program modules and/or devices drivers with access to the graphics circuitry 70. These program modules and/or devices drivers may, therefore, operate 30 in conjunction with graphics card 70 (e.g., send graphics related tasks to the graphics processor 350).

[0064] As indicated above, the graphics circuitry 70 and the display 10 engage in communication that adheres to the DDC2B standard. VESA, the Video Electronics Standards Association, developed the DDC2B standard, under which the graphics circuitry 70 is the master and the display 10 is the slave. Thus, under the DDC2B standard, the display 5 10 responds to requests and does not make requests or otherwise initiate transactions.

[0065] By using the I²C bus protocol, which was developed by Philips and is incorporated herein by reference, the DDC2B standard enables the graphics circuitry 70 to access data stored by the display 10. In particular, the DDC2B standard and the I²C bus protocol enable the graphics circuitry 70 to issue a request (as the master) to the display 10 for data, which 10 the display 10 subsequently transfers to the graphics circuitry 70. Previously, the graphics circuitry 70 requests such data during boot-up and configuration of the graphics circuitry 70 and/or electronic device 80. The data requested is stored in an I²C slave memory location (e.g., a location in the display memory 260). Additional transactions defined by the DDC2B standard include protocol synchronization and address offset specification.

15 [0066] The content and arrangement of at least some of the data stored by the display 10 and the data requested by the graphics circuitry 70 is preferably consistent with the Extended Display Identification Data ("EDID") standard. The EDID standard, at the time of this writing, has two versions that define separate data sets (e.g., EDID data sets) (both of which are incorporated herein by reference).

20 [0067] Of particular importance to embodiments that use an EDID version 1 data set are the 19th, 20th, and 127th bytes thereof. Bytes 19 and 20 disclose that the data set is an EDID version 1 data set. The 127th byte indicates whether additional data sets (e.g., an EDID version 2 data set) are also stored in the display memory 260 (e.g., data sets that do store orientation data). Of particular importance to embodiments that use an EDID version 2 data 25 set are the first byte, the 4th and 5th bits of the 82nd byte, and the 4th bit of the 85th byte. The first byte discloses that the data set is an EDID version 2 data set. The 4th and 5th bits of the 82nd byte disclose the orientation of the display 10 (e.g., whether the display 10 is in a portrait orientation or a landscape orientation). Similarly, the 4th bit of the 85th byte discloses whether the orientation of the display 10 is adjustable. In other words, whether the 30 orientation of the display 10 can be switched from landscape to portrait and vice versa (e.g., whether the present invention is applicable or not).

[0068] Moreover, the arrangement of data sets stored by the display 10 is preferably consistent with the Enhanced Extended Display Identification Data ("E-EDID™") standard, which is incorporated herein by reference. The use of the data sets and data set arrangement described in this and the two preceding paragraphs enables embodiments of the present invention to request and receive orientation information in a manner consistent with the DDC2B standard.

[0069] As stated above, the DDC2B standard defines a number of transactions. Of particular importance to the present invention is a data transfer. A data transfer is initiated by the graphics circuitry 70 and includes the display 10 transmitting data, such as orientation data, to the graphics circuitry 70.

[0070] To begin a data transfer, the graphics circuitry 70 transmits a start sequence, which indicates to the display 10 that data is about to be transmitted by the graphics circuitry 70. The graphics processor 250 typically transmits the start sequence by adjusting the data signal Pin/Skt 12 to a logic LOW state, and then adjusting the clock signal Pin/Skt 15 to a logic LOW state as illustrated in Figure 5A (i.e., by driving a high-to-low transition on the serial data line followed by a high-to-low transition on the serial clock line). Once the start sequence is transmitted, the data signal Pin/Skt 12 and the clock signal Pin/Skt 15 are not free until the graphics circuitry 70 transmits a stop sequence. The stop sequence may be transmitted by releasing the data signal Pin/Skt 12 to a logic HIGH state, and then releasing the clock signal Pin/Skt 15 to a logic HIGH state as illustrated in Figure 5B (i.e., by driving a low-to-high transition on the serial clock line followed by a low-to-high transition on the serial data line).

[0071] The graphics circuitry 70 then transmits an address. The address identifies the display 10. Figure 5C illustrates a series of data signal and clock signal transitions or states (i.e., bit values of one and zero) that comprise a transmission of the address and the read/write indicator.

[0072] As illustrated in Figure 5C, a bit value of one is transmitted by releasing the data signal Pin/Skt 12 to a logic HIGH state and holding the data signal Pin/Skt 12 at the logic HIGH state while adjusting the clock signal Pin/Skt 15 to a logic LOW state and subsequently releasing the clock signal Pin/Skt 15 to a logic HIGH state (e.g., a bit value of one is transmitted when the data signal is high while the clock signal has a low-to-high transition followed by a high-to-low transition). Further, a bit value of zero is transmitted by

adjusting the data signal Pin/Skt 12 to a logic LOW state and holding the data signal Pin/Skt 12 at the logic LOW state while adjusting the clock signal Pin/Skt 15 to a logic LOW state and subsequently releasing the clock signal Pin/Skt 15 to a logic HIGH state (e.g., a bit value of zero is transmitted when the data signal is low while the clock signal has a low-to-high transition followed by a high-to-low transition).

5 [0073] As also illustrated in Figure 5C, the address is typically 50 h and the read/write indicator (i.e., the least significant bit) is 0. By setting the read/write indicator to 0, the graphics circuitry 70 indicates that it will transmit an address offset in a subsequent byte of data.

10 [0074] After the graphics circuitry 70 transmits the address and the read/write indicator and the display 10 acknowledges them, the graphics circuitry 70 transmits an address offset (as defined in the DDC2B specification). The address offset identifies a location of a data set (e.g., an EDID version 1 data set, an EDID version 2 data set, etc.) maintained within the display memory 260 of the display 10. Typically, the address offset is 00 h, which as
15 indicated above may correspond to a first data set (e.g., an EDID version 1 data set) in a series of data sets maintained by the display 10. Upon receipt of the address offset, the display 10 then preferably stores this information within the display memory 260 for subsequent use. For example, the address offset may determine where the display controller
250 begins reading from the display memory 260 when responding to a subsequent request
20 for data by the graphics circuitry 70.

[0075] After the graphics circuitry 70 transmits the address offset and the display acknowledges them, the graphics circuitry 70 transmits the device address and the read/write indicator again (as defined in the DDC2B specification). This time, the read/write indicator is set to 1 to indicate that the graphics circuitry 70 is requesting 128 bytes of data beginning
25 at the address offset maintained by the display 10.

[0076] After the graphics circuitry 70 transmits the address and the read/write indicator and the display acknowledges them, the display 10 transmits data from the display memory 260 to the graphics circuitry 70 (as defined in the DDC2B specification). To do so, the display 10 modulates the state of the data signal Pin/Skt 12 to transmit data in a binary form (e.g., one
30 bit at a time). The graphics circuitry 70, however, continues to control the timing of the transmission by transmitting clock signal pulses. As defined by the DDC2B standard, the display 10 does not change or modulate the data signal Pin/Skt 12 while the clock signal

Pin/Skt 15 is in a logic HIGH state (doing so violates the DDC2B standard). The graphics circuitry 70 preferably samples or monitors the data signal Pin/Skt 12 while the clock signal Pin/Skt 15 is in the logic HIGH state. The graphics circuitry 70 acknowledges receipt of each byte of data. Similarly, the display 10 releases and monitors the data signal Pin/Skt 12 after transmitting each byte of data, with the exception of the last byte of data, to confirm the graphics circuitry's 70 acknowledgment. Following each acknowledgment, the display 10 transmits a subsequent byte of data. And after all of the data has been transmitted and acknowledged, the display 10 transmits a checksum, which may be used for transmission error detection. If an error occurs, the data may be requested an additional time. The graphics circuitry 70 responds to the checksum with a not acknowledge (i.e., a NACK) by allowing the data signal Pin/Skt 12 to float to a logic HIGH state and transmitting a clock signal pulse. The graphics circuitry 70 may, for example, then transmit a stop sequence or transmit another DDC2B standard command (e.g., address offset specification, data request, etc.).

[0077] Figure 6 illustrate a series of steps taken by the graphics circuitry 70 and the display 10 consistent with an embodiment of the present invention. These processing steps preferably take place after the display 10 and the graphics circuitry 70 achieve protocol synchronization, which is described in detail in the DDC2B specification and is beyond the scope of the present invention. In a first step (state or series of steps) (by the graphics circuitry 70), the graphics circuitry monitors the data signal Pin/Skt 12 and the clock signal Pin/Skt 15 (step 642). As described above, the graphics circuitry 70 may include input buffers connected to the data signal Pin/Skt 12 and the clock signal Pin/Skt 15, respectively. The data signal Pin/Skt 12 and the clock signal Pin/Skt 15 should be in a logic HIGH state (due to, for example, various pull-up resistors) during periods of inactivity. The graphics circuitry 70 may monitor the data signal Pin/Skt 12 and the clock signal Pin/Skt 15 by, for example, periodically checking the value of these input buffers. The graphics circuitry 70 may also continuously monitor these signals for state transitions (i.e., signal edges).

[0078] If the graphics circuitry 70 does not detect a signal modulation (step 643-No), the graphics circuitry 70 continues to monitor the data signal Pin/Skt 12 and the clock signal Pin/Skt 15.

[0079] While the graphics circuitry 70 monitors the data signal Pin/Skt 12 and the clock signal Pin/Skt 15, the orientation detector 270 monitors the orientation of the display 10 (step

644). If the orientation detector 270 does not detect a change to the orientation of the display 10 (step 646-No), the orientation detector 270 continues to monitor the orientation of the display 10.

[0080] But if the orientation detector 270 detects a change to the orientation of the display

5 10 (step 646), the display controller 250 updates orientation data maintained in the display memory 260. More specifically, the display controller 250 receives orientation input from the orientation detector 270 as described above and, for example, updates the 4th and 5th bits of the 82nd byte of an EDID version 2 data set maintained in the display memory 260 to reflect the new orientation of the display 10.

10 [0081] The display controller 250 then modulates the data signal Pin/Skt 12 and/or the clock signal Pin/Skt 15. As described above, the display 10 is a slave device. As a result, the display 10 should not modulate the data signal Pin/Skt 12 (i.e., transmit data) unless the graphics circuitry 70 makes a request for data or modulate the clock signal Pin/Skt 15 under any circumstances.

15 [0082] So if an orientation change is detected by the orientation detector 270, the display 10 may transmit a pulse over the data signal Pin/Skt 12. In other words, the display 10 may adjust the data signal Pin/Skt 12 to a logic LOW state, hold the data signal Pin/Skt 12 in this state for a defined period of time, and then allow the data signal Pin/Skt 12 to float back to a logic HIGH state. As noted above, the DDC2B standard does not permit the display 10 to

20 adjust the data signal Pin/Skt 12 while the clock signal Pin/Skt 15 is in a logic HIGH state. The graphics circuitry 70 will detect this data pulse (as described above), and take some or all of steps 654-667, which are described in detail below. Other devices detecting this pulse will ignore it since this pulse was not requested and is not defined or allowed by the DDC2B standard (e.g., does not comprise a start sequence).

25 [0083] In embodiments in which the graphics circuitry 70 continuously transmits clock signal pulses, the display 10 times modulation of the data signal Pin/Skt 12 to coincide with the clock signal Pin/Skt 15 being in a logic HIGH state, as illustrated in Figure 7A. As shown in Figure 7A, the modulation 700 of the data signal Pin/Skt 12 takes place while the clock signal Pin/Skt 15 is in a logic HIGH state 702 (the use of the third time slot or clock

30 pulse is arbitrary).

[0084] In embodiments in which the graphics circuitry 70 does not continuously transmit clock signal pulses, the display 10 modulates the data signal Pin/Skt 12 at anytime, as

illustrated in Figure 7B. As shown in Figure 713, the modulation 704 of the data signal Pin/Skt 12 takes place while the clock signal Pin/Skt 15 is in a logic HIGH state 706. Subsequently, the graphics circuitry 70 initiates a request for data from the display 10 by transmitting a start signal, which is done by pulling data signal Pin/Skt 12 low 708, followed 5 by pulling clock signal Pin/Skt 15 low 710, subsequently followed by transmissions according to the DDC2B standard.

[0085] In some embodiments, the modulation indicating a change in the orientation of the display 10 takes the form of an illegal pulse (or "glitch") on the data signal Pin/Skt 12, as exemplified by 700 and 704 in the figures. According to the standards incorporated above, 10 this type of pulse is illegal, but is used by the present invention to signal an orientation change of the display 10.

[0086] In still other embodiments, the display 10 transmits a pulse over the clock signal Pin/Skt 15 if an orientation change is detected by the orientation detector 270. In other words, the display 10 may adjust the clock signal Pin/Skt 15 to a logic LOW state, hold the 15 clock signal Pin/Skt 15 in this state for a defined period of time, and then allow the clock signal Pin/Skt 15 to float back to a logic HIGH state. The graphics circuitry 70 will detect this pulse, and take some or all of steps 654-667, which are described in detail below. As noted above, the DDC2B standard does not permit the display 10 to modulate the clock signal pulse. Other devices detecting this pulse will ignore it since this pulse was not requested and 20 is not defined or allowed by the DDC2B standard (e.g., does not comprise a start sequence).

[0087] Other data and/or clock signals that are undefined or illegal operations under the DDC2B standard are possible and within the scope of the present invention. For example, the display 10 may transmit a start sequence, an invalid address (e.g., fewer than a prescribed number of address bits or an illegal/undefined combination of bits), and then a stop sequence. 25 Again, the graphics circuitry 70 is the master of the data and clock signals so no activity should take place without a request from the graphics circuitry 70. The graphics circuitry 70, therefore, preferably responds to this activity as described below. But other devices detecting this activity will ignore it since an invalid address (according to the DDC2B standard) is specified.

30 [0088] The graphics circuitry 70 should detect the modulation of the data signal Pin/Skt 12 and/or the clock signal Pin/Skt 15 (by catching signal edges or periodic sampling of the signals) (step 643-Yes) and respond by requesting orientation data from the display 10 (step

654). As described in detail above, this typically includes transmitting a start sequence, an address offset, a request for data at the specific address, and a stop sequence. The display 10 preferably responds by acknowledging the request and serially transmitting the data as described above.

5 [0089] Upon receiving the data, the graphics circuitry 70 extracts the orientation information from the data set (step 662). If the extracted orientation information indicates that the orientation of the display 10 has not changed (e.g., the orientation of the display 10 is consistent with the current formatting of display data 85 transmitted by the graphics circuitry 70) (step 664-No), the graphics circuitry 70 takes no further action with respect to the signal modulation detected in step 652 and continues to monitor the data and clock signals for a signal modulation (step 642). But if the extracted orientation information indicates that the orientation of the display 10 has changed (step 664-Yes), the graphics circuitry 70 formats the display data 85 accordingly (step 667) and then continues to monitor the data and clock signals for another signal modulation (step 642).

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15 [0090] While the present invention has been described with reference to a few specific embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims. In the claims, the order in which steps or operations are listed does not imply any order in

20 which the steps or operations are to be performed, unless specifically stated in the claim.